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A 2D material-based floating gate device with linear synaptic weight update†

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Neuromorphic computing is of great interest among researchers interested in overcoming the von Neumann computing bottleneck. A synaptic device, one of the key components to realize a neuromorphic system, has a weight that indicates the strength of the connection between two neurons, and updating this weight must have linear and symmetric characteristics. Especially, a transistor-type device has a gate terminal, separating the processes of reading and updating the conductivity, used as a synaptic weight to prevent sneak path current issues during synaptic operations. In this study, we fabricate a top-gated flash memory device based on two-dimensional (2D) materials, MoS_2 and graphene, as a channel and a floating gate, respectively, and Al_2O_3 and HfO_2 to increase the tunneling efficiency. We demonstrate the linear weight updates and repeatable characteristics of applying negative/positive pulses, and also emulate spike timing-dependent plasticity (STDP), one of the learning rules in a spiking neural network (SNN).

1. Introduction

As interest in AI (artificial intelligence) has grown, quick and accurate calculations are needed to process massive amounts of data for the perception of language, images and sound.[1–4] However, in the current von Neumann-based computing architecture, a data bus between the CPU and memory to process information has been the main bottleneck in high-speed and low-power computing for big data. In this regard, neuromorphic computing, which mimic the human brain, has become one of the most viable methods in future computing systems.[5] A neuromorphic system mainly consists of two different types of devices, neurons and synapses.[6,7] A synapse plays an important role in transporting information from a pre-synaptic neuron to a post-synaptic neuron. A synapse contains weight information, which is altered when neuronal activity changes the strength of the connections between the neurons. In neuromorphic computing, the weight is typically expressed as the conductance level of the synaptic device.

Two-terminal devices, such as memristors (ReRAM, PCRAM, *etc.*),[2,8–10] have been introduced as promising candidates for artificial synapses. A memristor, as the name suggests, acts as a memory resistor. However, in the formation of an array for an artificial neural network using two-terminal memristors, unwanted leakage current through the sneak path becomes one of the major issues standing in the way of system implementation. Many studies have suggested ideas to circumvent this issue, such as using additional selector devices like transistors, diodes, and OTS devices[8,11,12] or applying complicated pulse inputs.[13]

Recently, three-terminal-based synaptic devices have become more popular in an effort to solve this issue.[14] A gate of a three-terminal device controls and separates the weight updating and reading paths, effectively preventing the sneak path problem.[15] Also, the absence of an additional selector device, which is required for a two-terminal-based synaptic array, helps reduce the total chip area. Given the aforementioned advantages, flash memory devices have become promising candidates as synaptic devices. Although several flash-type synaptic devices, including silicon,[16] CNT (carbon nanotube),[15] and TMDC (transition metal dichalcogenide)-based

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flash devices,[17,18] suggest improvements in the characteristics of synaptic devices, a top-gated flash memory device based on 2D materials has not been intensively studied in terms of its adequacy as a synaptic device.[19–21]

In this work, we fabricated top-gated floating gate synaptic devices based on two-dimensional (2D) materials using MoS_2 for the device channel and graphene for the floating gate. MoS_2 has been extensively studied as a future semiconductor material; it has a large band gap of 1.2 eV for bulk and 1.8 eV for single-layer,[22,23] and also shows excellent thermal and ambient stability with a high electrostatic integrity.[24,25] Graphene has a high density of states and high work function, making it suitable as a floating gate.[14] We used MOCVD-grown MoS_2 and CVD-grown graphene to show their potential for a large-scale neuromorphic array. The main operating mechanism of flash memory is based on trapping/de-trapping of the electrons in the floating gate. For its operation, a sufficiently high voltage pulse is applied to the top gate electrode (V_{tg}), which forms the tunneling voltage (V_{tunnel}) across the tunneling oxide due to the device coupling ratio (basically, a capacitive divider defined as $C_{block}/(C_{tunnel} + C_{block})$ where C_{block} is the capacitance between the top gate and the floating gate and C_{tunnel} is the capacitance between the floating gate and the channel). Since a high coupling ratio improves the tunneling efficiency, a properly designed gate stack is necessary. We used HfO_2 ($k \sim 25$) as the blocking oxide and Al_2O_3 ($k \sim 10$) as the tunneling oxide with different thicknesses to improve the coupling ratio.[26]

In highly efficient neuromorphic computing, several synaptic device properties, such as multilevel weight states (multi-conductance levels), asymmetry and non-linearity, power consumption, and the variability of the synaptic device, must be considered.[6,27] As shown in previous studies, the capacity for high-conductance states with good linear synaptic update leads to better learning capability and improved network robustness.[6,12,28–31] We demonstrate that our flash-type synaptic device improves the non-linearity of the synaptic weight by improving the tunneling efficiency of the device. In addition, for the first time, we are able to emulate spike timing-dependent plasticity (STDP) in a 2D material-based top-gated floating gate device to show the possible utility of a SNN-based neuromorphic computing system.

2. Results and discussion

Fig. 1a shows a schematic illustration of our flash-type memory device structure where MoS_2 is used for the channel, and the graphene floating gate is separated from the channel by Al_2O_3 tunneling oxide. Graphene has a work function of 4.6 eV and acts as a deep potential well for charge trapping. The conductivity of the MoS_2 channel depends on the amount of charge stored in the floating gate, which is controlled by the gate voltage pulse. MOCVD-grown few-layer MoS_2 film[32] was transferred onto the target wafer using a wet transfer method. The target wafer consisted of highly-doped p-type Si with thermally grown 300 nm SiO_2. Then, the few-layer MoS_2 was etched by O_2 cleaner or reactive ion etching to form a channel. Ti/Au electrodes with thicknesses of 5 nm/100 nm, respectively, were deposited by e-beam evaporation for the source and drain contacts. Here, Ti served as an adhesion layer. Subsequently, the device was annealed at 300 °C in a 5% forming gas of H_2/N_2 for 2 hours. During this annealing process, PMMA residues from the wet transfer process, photoresist residues, and other contaminants on the sample surfaces were removed. As the high coupling ratio improves the tunneling efficiency and the non-linearity of the synaptic weight updates of the device (Fig. S1 in the ESI†), the gate

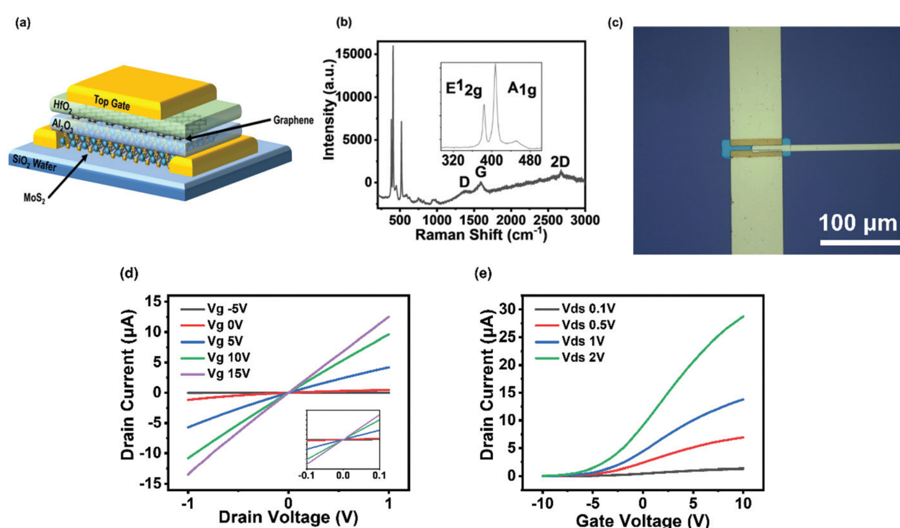

Fig. 1 Top-gate floating gate memory. (a) Schematic of the fabricated device. MoS_2 and graphene serve as the channel and floating gate, respectively. (b) Raman spectrum of MoS_2 and graphene. (c) Optical image of the device; scale bar, 100 μm. (d) The output characteristics ($I_{ds} - V_{ds}$) of the device with various top-gate voltages. The inset shows the output characteristics in a narrow V_{ds} range indicating ohmic contact. (e) Transfer characteristics at various drain voltages. These findings show the n-type behavior of the device.

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stack was properly designed. A tunneling oxide of 10 nm Al_2O_3 was first deposited by an ALD process at 150 °C. The MoS_2 encapsulated by the high-k material improved the device performance by reducing Coulomb scattering and fixed phonon dispersion in the MoS_2 channel.[33–35] Next, the CVD-grown few-layer graphene film on Cu foil was transferred again using the wet transfer method. Graphene and MoS_2 were identified by Raman spectroscopy using a confocal Raman microscope with a 532 nm laser and ×50 objective lens. The diameter size of the laser beam was ∼2 μm and the output power was ∼5 mW. The Raman peaks of both MoS_2 (E^1_{2g} and A_{1g})[36] and graphene (D, G and 2D)[37] are shown in Fig. 1b. Finally, the blocking oxide of 20 nm HfO_2 and top gate electrode (Ti/Au 5 nm/100 nm) were deposited by ALD and E-beam evaporation, respectively. An optical image of the final device is shown in Fig. 1c.

Fig. 1d and e show the *IV* curves of the fabricated synaptic device. The output characteristics ($I_{ds} - V_{ds}$) of the device are shown in Fig. 1d. The output curve was measured from −1 to +1 V in 5 mV steps under different V_{tg} bias conditions (−5 to +15 V with 5 V steps), and shows clear gate modulation. The inset of the output curve (Fig. 1d) indicates that the device contacts formed ohmic contacts. Fig. 1e shows the transfer curve of one of the fabricated devices. The fabricated device exhibits n-type behavior that is always ON in the positive drain bias region. The transfer curve was obtained by sweeping the V_{tg} from −10 to +10 V in 100 mV steps while V_{ds} was gradually increased from 0.1 to 2 V. The field effect mobility of the device was 3.07 $cm^2\ V^{-1}\ s^{-1}$ as calculated from eqn (1):[12,25]

$$\mu = \left(\frac{\mathrm{d}I_{ds}}{\mathrm{d}V_{tg}}\right) \times \left[\frac{L}{WC_iV_{ds}}\right] \tag{1}$$

where L and W are the channel length (5 μm) and width (5 μm), respectively, and C_i is the capacitance between the channel and top gate per unit area (series capacitance of 10 nm Al_2O_3 and 20 nm HfO_2, $C_i = 4.92 \times 10^{-3}\ F\ m^{-2}$). Additional transfer curves with different V_{tg} sweeping ranges that were measured to gauge memory behavior with hysteresis are available in the ESI (Fig. S2†).

To mimic potentiation and depression of a biological synapse, two voltage pulse trains were sequentially applied to the gate electrode to update the weight, and the device drain current was read after each pulse was applied.[17,38–41] Here, the voltage pulse applied to the gate represented a neuronal spike and the measured drain current represented the synaptic weight. In the floating gate device, application of a positive voltage pulse to the control gate resulted in charge trapping in the channel. When the floating gate was charged with electrons, this trapped charge screened the gate electric field, thus increasing the threshold voltage. On the other hand, application of a negative voltage pulse to the gate effectively removed the trapped charges from the floating gate and, in turn, decreased the threshold voltage. In the experiment, thirty-five negative voltage pulses were first applied to the gate for potentiation (increasing the drain current), then thirty-five positive pulses were applied for depression (decreasing the drain current). The applied pulse amplitudes were −10 V with 1 μs pulse width and +8 V with 1 μs pulse width, respectively, followed by drain current read operation (V_{tg} = 0 V and V_{ds} = 0.1 V) after applying each pulse.

According to Chen *et al.*, non-linearity of the potentiation and depression updates in a synaptic device is one of the keys to achieving high accuracy in a neuromorphic system.[6] The non-linearity factor is derived from eqn (2) and (3):[29]

Potentiation:

$$G_{pot} = G_1(1 - e^{-\nu P}) + G_{min} \tag{2}$$

Depression:

$$G_{dep} = G_{max} - G_1(1 - e^{-\nu(1-P)}) \tag{3}$$

where

$$G_1 = \frac{G_{max} - G_{min}}{1 - e^{-\nu}}$$

G_{max} and G_{min} are the maximum and minimum conductance, respectively, and ν is a parameter of non-linearity. P is the normalized pulse number. Our 2D material-based top-gated synaptic device shows non-linearities of 1.83 for the potentiation curve and 1.88 for the depression curve while having thirty-six synaptic weight states (Fig. 2a). To the best of our knowledge, these are the lowest non-linearity values yet reported in this type of device. Furthermore, our device exhibited linear and repeatable potentiation and depression behaviors when negative and positive pulses were repeatedly applied (1330 pulses), indicating the robustness of the device (Fig. 2b). The average non-linearity values from the multicycle experiment are 1.94 and 2.22 for potentiation and depression, respectively (Fig. 2c).

Fig. 3 illustrates the energy band diagrams of the device that demonstrate the device's operating principles. The respective energy bandgap (E_g) and electron affinity (χ) values are approximately 1.2 and 4.3 eV for the few-layer MoS_2,[42] 6.8 and 1.35 eV for Al_2O_3, and 5.25 and 2.0 eV for HfO_2.[43] The electron affinity of graphene is 4.26 eV.[44,45] The barrier height for electron tunneling from the MoS_2 channel to the graphene floating gate through the Al_2O_3 layer is approximately 3 eV (Fig. 3a). When a high positive voltage pulse (the depression operation of the synaptic update) was applied to V_G ($V_G > 0$), electrons were able to tunnel from MoS_2 to the graphene floating gate through Al_2O_3. The thickness of the blocking oxide (HfO_2) prevented tunneling to the top gate. The tunneled electrons that accumulated in the graphene floating gate screened the top gate electric field, resulting in a positive V_{th} shift and a decrease in conductance (Fig. 3b). On the other hand, when a negative voltage pulse (the potentiation operation of the synaptic update) was applied to V_G ($V_G < 0$), electrons were transferred back from the graphene floating gate to the MoS_2 channel, resulting in a negative V_{th} shift and an increase in the conductance (Fig. 3c).

Furthermore, we modulated the applied pulse conditions to examine the synaptic weight updates in various cases since the

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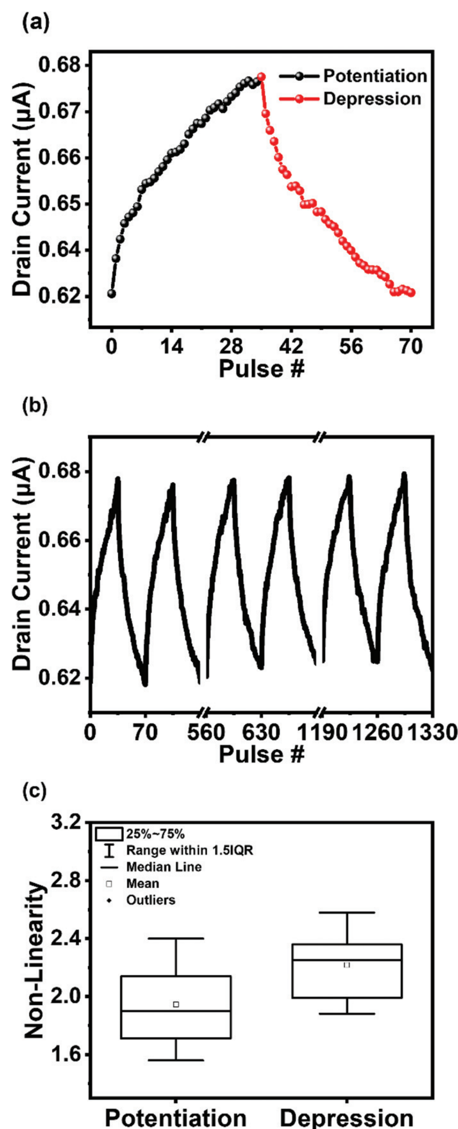

Fig. 2 (a) Current modulation with negative and positive voltage pulses. Pulses of −10 V with 1 μs pulse width and +8 V with 1 μs pulse width were applied thirty-five times each. (b) The results of 19 cycles of potentiation and depression. These findings show the robustness of the device during the synaptic operation. (c) The box-plot of non-linearity values is shown. The average values of potentiation and depression are 1.94 and 2.22, respectively.

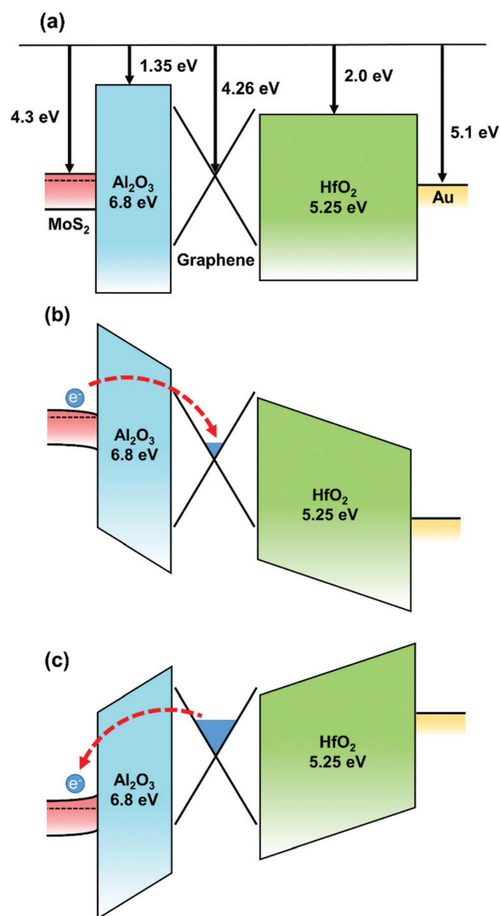

Fig. 3 Band diagram of the device. (a) Flat band diagram. (b, c) Band diagram when bias is applied at the top gate. Fig. 4b represents the state when positive voltage is applied. Fig. 4c shows the state when negative voltage is applied.

modulations of pulse width and amplitude have effects on electron tunneling, and therefore, the synaptic weight changes. Fig. 4a shows the results of using four different pulse widths (1, 5, 10, and 20 μs) with a pulse amplitude of −10 V for potentiation and +8 V for depression. Ten pulse cycles were applied in each case. From Fig. 4b and c, non-linearity increases with increasing pulse width in both potentiation and depression. Different amplitudes were also tested (Fig. S3 in the ESI†) and we observe that the amount of weight change increases for the higher pulse amplitude.

Since previous studies reported that a higher number of conductance levels (weight bits) in a synaptic device improves the learning accuracy in a neural network,[6,27] we examined the effect of the number of synaptic weight levels on the non-linearity of our device. As seen in Fig. 4d, four different conductance levels (35, 50, 75 and 100) under the same pulse width and amplitude conditions used in Fig. 2 were tested in our device. From Fig. 4e and f, the extracted non-linearity values remained around 2 regardless of the weight levels, implying that our device is applicable to various neuromorphic systems with different number of weight update levels.

In addition, we studied the synaptic plasticity of the device by demonstrating STDP behavior. STDP is a popular learning rule in spiking neural networks (SNNs); it modulates synaptic weights according to the difference in spike timing between a pre-synaptic neuron (V_{pre}) and a post-synaptic neuron (V_{post}).[10,46,47] To demonstrate STDP behavior, we applied a set of multiple differently shaped pulses, which contained information about the timing difference between the V_{pre} and V_{post} spikes, to the top gate voltage. The pulse shapes of V_{pre} and V_{post} were adapted from a previous study.[10] According to this study, these two pulses have the same shape but arrive at two

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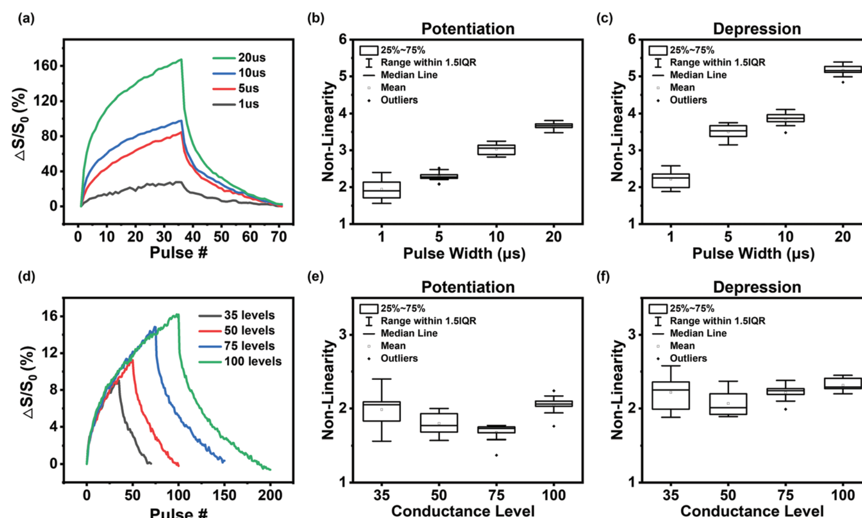

Fig. 4 (a) Results of various applied pulses when pulse width is modulated. (b, c) Non-linearity values of potentiation/depression at various pulse widths. (d) Measurements taken at four conductance levels. (e, f) Extracted non-linearity values of potentiation/depression. The value remains near 2 regardless of the number of conductance levels.

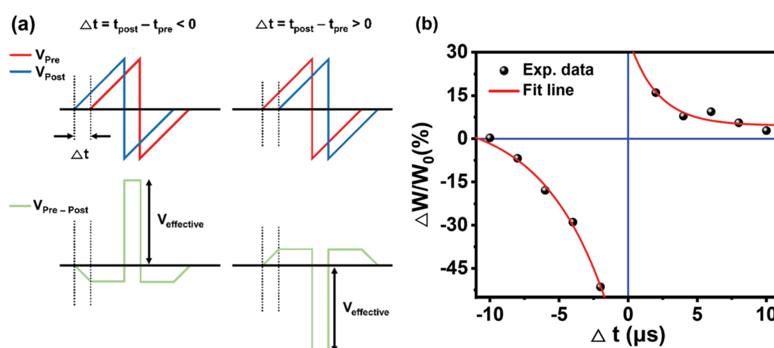

Fig. 5 (a) The shapes of the pre- and post-synaptic pulses used to calculate the actual applied pulse are shown along with the calculation results. (b) STDP results at various time differences. The dots show the experimental data and the fit line is shown in red.

different time points (t_{pre} and t_{post}), with various time differences ($\Delta t = t_{post} - t_{pre}$). The summation of V_{pre} and V_{post} (applied voltage $V_{applied} = V_{pre} - V_{post}$) was applied to our device as represented in Fig. 5a. When Δt was greater than 0, the positive portion of $V_{applied}$ always had a low amplitude, while the negative portion of $V_{applied}$ had an amplitude large enough to change the current value (synaptic weight) of the device. Likewise, when Δt was greater than 0, the negative portion of $V_{applied}$ had a low amplitude that could not readily change the weight, while the positive portion had a large amplitude causing weight change. In both cases, the effective part ($V_{effective}$) that changed the weight was positive when $\Delta t < 0$ and negative when $\Delta t > 0$, and it took as much time as Δt. The STDP results can be seen in Fig. 5b. The dots show the amount of conductance change at each Δt, and the red line indicates that the results can be fitted as an exponential decay function at both polarities. In both polarities, the shorter the Δt, the greater the amount of weight change.

3. Conclusion

In conclusion, top-gated flash memories based on CVD-grown 2D materials for a synaptic device were fabricated and the synaptic characteristics were investigated, which successfully demonstrated biological synaptic behaviors (linear synaptic weight updates and STDP). The device exhibited non-linearities in potentiation and depression of about 1.9 and 2.2, respectively. The repeated measurements taken after consecutive application of 1330 pulses ensure the robustness of the device for numerous synaptic updates during the operation. In addition, the STDP results suggest that the synaptic device is applicable to a SNN-based neuromorphic hardware system. By using CVD-grown 2D materials, we also demonstrate the possibility of building a large-scale neuromorphic computing array. These results show that 2D material-based top-gated flash memory is an excellent candidate for neuromorphic computing.

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4. Experimental section

MoS_2 film growth

The few-layer MoS_2 film was grown on a Si/SiO_2 (300 nm) substrate *via* metal–organic chemical vapor deposition (MOCVD). Our MOCVD reactor consists of a 4.3-inch quartz tube and a 3-zone heating furnace. We used molybdenum hexacarbonyl (MHC: Sigma-Aldrich 577766, >99.9% purity) and diethyl sulfide (DES: Sigma-Aldrich 107247, >98%) as the transition metal and chalcogen precursors, respectively. The pressure of both precursors in bubblers was kept constant at 800 Torr, and the temperature of the MHC canister was constantly kept at 60 °C. The optimum flow rates of MHC, DES, H_2, and Ar for the growth of few-layer MoS_2 were 0.6 sccm, 1.2 sccm, 5 sccm, and 1000 sccm, respectively, where the kinetics of the precursor decomposition controlled the thickness of MoS_2 film. The flow rates of precursors and gases were precisely regulated by mass flow controllers (MFCs). The 3-zone furnace was heated to the growth temperature of 450 °C, 600 °C, 600 °C for 50 min under H_2 and Ar atmosphere. The MoS_2 growth was performed at 3.7 Torr for 14 hours. The substrate, which was placed on a quartz plate, was loaded at the central zone of the furnace. NaCl was placed on the quartz plate at the upstream region of the furnace to control the grain size and intergrain connection of MoS_2 films.

2D material film transfer process

2D material films (MOCVD-grown MoS_2 on SiO_2/Si substrate and CVD-grown graphene on Cu foil) were first spin-coated with polymethyl methacrylate (PMMA), followed by baking at 170 °C for 2 minutes. For MoS_2 transfer, the $PMMA/MoS_2/SiO_2/Si$ stack was soaked in deionized water (DI water) to separate the $PMMA/MoS_2$ film from the substrate. The film was stripped off from the edge of the substrate by a tweezer under water. The film was then transferred onto the target substrate, followed by heating at 70 °C for 10 min on the hot plate to remove water and ensure good adhesion between the film and the substrate. Subsequently, PMMA was removed by immersion in acetone for 2 hours and then dried with N_2 gas. For graphene transfer, the PMMA/graphene/Cu foil stack was floated on the copper etchant for 2 hours to remove the Cu foil portion. Then, the stack was transferred to a clean wafer multiple times to rinse off the Cu etchant residues. Finally, the fully rinsed PMMA/graphene stack was transferred onto the target substrates, followed by the PMMA removal process.

Material characterizations

The morphology of the samples was characterized by optical microscopy (Olympus, BX53). The two types of 2D materials (graphene, MoS_2) were characterized by Raman microscopy (Renishaw, InVia Raman Microscope, Yag laser 532 nm wavelength).

Device fabrication and measurement

Top-gate flash memory devices were fabricated on a highly p-doped SiO_2/Si wafer by photolithography using a mask aligner (SUSS microtec, MA6). The metal electrodes (5 nm Ti and 100 nm Au) were deposited by an electron beam evaporator (Korea Vacuum Tech, KVE-2004). 10 nm of Al_2O_3 for tunneling oxide and 20 nm of HfO_2 for blocking oxide were deposited using an atomic layer deposition system (Veeco, Savannah S200). Electrical properties (transfer characteristics, output curve, potentiation–depression, and STDP) were measured by a cryogenic probe station (MS Tech, M5VC) and a semiconductor tester (Keithley, 4200A-SCS) at room temperature and normal pressure.

Author contributions

E. P. conceived and designed the research and drafted the manuscript under the supervision of J. C., K. K., and J. Y. K., M. K. and I. K. prepared graphene and ALD oxides. T. K. prepared MoS_2 film. J. P., J. K., Y. J., S. L., I. K., J. P., and G. K. participated in the design of the study and data analysis. All the authors discussed the results and commented on the manuscript.

Conflicts of interest

The authors declare no conflict of interest.

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